IN THE CLAIMS:

Please **AMEND** claim 12-23 and 25-36 as follows.

1. (Previously Presented) A method for detecting an assumed octet slip in an inband signalling block in pulse code modulation, the method comprising:

searching a first error at a position bit k1 starting from an end of a searching block, the searching block comprising a set of bits;

counting a number of bit errors starting from a corresponding position k1 in a slipped block, the slipped block being another set of bits where each bit is shifted relatively to a corresponding bit of the searching block; and

detecting octet slip by analyzing the error bits.

2. (Original) The method according to claim 1, wherein when the chosen direction is from a first bit to a last bit, the searching block is a signalling block and the slipped block is adjacent block.

3. (Original) The method according to claim 1, wherein when the chosen direction is from a last bit to a first bit, the searching block is an adjacent block and the slipped block is a signalling block.

4. (Original) The method according to claim 3, further comprising verifying a correctness of the signalling block before searching.

5. (Original) The method according to claim 2 , wherein searching and counting bit errors is performed by comparing the signalling block and the adjacent block to a sample block.

6. (Original) The method according to claim 2, wherein the octet slip is detected starting from or after the bit k1 if the number of the bit errors in the slipped block is more than one.

7. (Original) The method according to claim 2, wherein the octet slip is detected before the bit k1 if the number of error bits starting from the bit k1 is zero or one.

8. (Original) The method according to claim 6, further comprising searching a second error bit k2 of the searching block starting from a bit after the first error bit k1.

9. (Original) The method according to the claim 8, further comprising detecting if the bits of the slipped block starting from the second error bit k2 are correct.

10. (Original) The method according to the claim 9, further comprising detecting that the octet slip between the error bits k1 and k2 and the number of bit errors is one if the bits in the slipped block starting from the second error bit k2 are correct.

11. (Original) The method according to the claim 9, further comprising determining that the octet slip cannot be detected if the number of bit errors is more than one.

12. (Currently Amended) A device for detecting an assumed octet slip in an inband signalling block in pulse code modulation comprising a slip detector, the device comprising:

a searcher ~~arranged~~ configured to search a first error bit at a position k1 starting from an end of a searching block, the searching block comprising a set of bits;

a counter configured ~~arranged~~ to count a number of bit errors starting from a corresponding po9sition k1 in a slipped block, the slipped block being another set of bits where each bit is shifted relatively to a corresponding bit of the searching block; and

a detector configured ~~arranged~~ to detect the octet slip by analyzing error bits.

13. (Currently Amended) The device according to claim 12, wherein if the chosen direction is from a first bit to a last bit the device is configured ~~arranged~~ to set the

searching block to correspond to a signalling block and the slipped block to correspond to an adjacent block.

14. (Currently Amended) The device according to claim 12, wherein if the chosen direction is from a last bit to a first bit the device is configured ~~arranged~~ to set the searching block to correspond to an adjacent block and the slipped block to correspond to a signalling block.

15. (Currently Amended) The device according to claim 14, wherein the device is configured ~~arranged~~ to verify a correctness of the signalling block before searching.

16. (Currently Amended) The device according to claim 13, wherein the searcher is configured ~~arranged~~ to search bit error by comparing the signalling block and the adjacent block to a sample block.

17. (Currently Amended) The device according to claim 13, wherein the detector is configured ~~arranged~~ to detect the octet slip starting from or after the bit k1, if the number of bit errors in the slipped block is more than one.

18. (Currently Amended) The device according to claim 13, wherein the detector is configured ~~arranged~~ to detect the octet slip before the bit k1 if the number of bit errors starting from the bit k1 is zero or one.

19. (Currently Amended) The device according to claim 17, wherein searcher is configured ~~arranged~~ to search a second error bit k2 of the searching block starting from a bit after the first error bit k1.

20. (Currently Amended) The device according to the claim 19, wherein the detector is configured ~~arranged~~ to detect if bits of the slipped block starting from the second error bit k2 are correct.

21. (Currently Amended) The device according to the claim 20, wherein the detector is configured ~~arranged~~ to detect that the octet slip between the error bits k1 and k2 and the error count is one if the bits starting from the error bit k2 are correct.

22. (Currently Amended) The device according to the claim 21, wherein the detector is ~~arranged~~ configured to determine that the octet slip cannot be detected if the number is more than one.

23. (Currently Amended) A system for detecting an assumed octet slip in an inband signalling block in pulse code modulation, which system comprises:

a sender terminal configured to transmit a signal;

a receiver terminal;

an in path equipment; and

a slip detector ~~that is arranged to detect assumed octet slip, the slip detector~~ comprising~~,~~

a searcher configured ~~arranged~~ to search a first error bit at a position k1 starting from an end of a searching block, the searching block comprising a set of bits,

a counter configured ~~arranged~~ to count a number of bit errors starting from a corresponding position k1 in a slipped block, the slipped block being another set of bits where each bit is shifted relatively to a corresponding bit of the searching block, and

a detector configured ~~arranged~~ to detect the octet slip by analyzing error bits,

wherein the slip detector is configured to detect assumed octet slip of the signal transmitted from the sender terminal through the in path equipment to the receiver terminal.

24. (Cancelled)

25. (Currently Amended) The system according to claim 23, wherein if the chosen direction is from a first bit to the last bit the device is configured ~~arranged~~ to set the searching block to correspond to a signalling block and the slipped block to correspond to an adjacent block.

26. (Currently Amended) The system according to claim 23, wherein if the chosen direction is from a last bit to a first bit the device is ~~arranged~~ configured to set the searching block to correspond to an adjacent block and the slipped block to correspond to a signalling block.

27. (Currently Amended) The system according to claim 26, wherein the device is ~~arranged~~ configured to verify a correctness of the signalling block before searching.

28. (Currently Amended) The system according to claim 25, wherein the searcher is ~~arranged~~ configured to search bit error by comparing the signalling block and the adjacent block to a sample block.

29. (Currently Amended) The system according to claim 25, wherein the detector is arranged to detect the octet slip starting from or after the bit k1, if the number of the bit errors in the slipped block is more than one.

30. (Currently Amended) The system according to claim 25, wherein the detector is configured ~~arranged~~ to detect the octet slip before the bit k1 if the number of bit errors starting from the bit k1 is zero or one.

31. (Currently Amended) The system according to claim 29, wherein the searcher is configured ~~arranged~~ to search a second error bit k2 of the searching block starting from a bit after the first error bit k1.

32. (Currently Amended) The system according to claim 31, wherein the detector is configured ~~arranged~~ to detect if the bits of the slipped block starting from the second error bit k2 are correct.

33. (Currently Amended) The system according to claim 32, wherein the detector is ~~arranged~~ configured to detect that the octet slip between the error bits k1 and k2 and the number of bit errors is one if the bits starting from the error bit k2 are correct.

34. (Currently Amended) The system according to claim 33, wherein the detector is configured ~~arranged~~ to determine that the octet slip cannot be detected if the number is more than one.

35. (Currently Amended) The system according to claim 23 wherein the slip detector is configured ~~arranged~~ into the path equipment.

36. (Currently Amended) The system according to the claim 23, wherein the slip detector is configured ~~arranged~~ into the receiver terminal.